REMARKS

Claims 38 and 43 have been amended.

The Examiner has rejected applicants' claims 38-43 under 35 USC §112, first paragraph as failing to comply with the enablement requirement. In this regard, the Examiner has argued that the specification does not describe "an first encoder for encoding a first digital information and output parallel data of L bits and first converting for converting into parallel data of L bits into the first parallel data of N bits and an error correcting unit for adding the error correcting coded into the first parallel data as being recited in claims 38-43." The Examiner further notes that "the specification teaches only the MUSE signal is processed into parallel data."

In order to avoid this rejection, applicants have amended independent claims 38 and 43 as above set forth. In particular, the term "parallel data " has been changed to --data-- in the claims so that the claims are now believed to be supported by the embodiment of applicants' invention shown in FIG. 12.

More particularly, looking at applicants' amended claim 38, it recites a first encoder arranged to encode the first digital information data and output data of L bits, a second encoder, arranged to encode the second digital information data and output data of M bits, where $L \neq M$, a first converter, arranged to generate first data of N bits by using a plural of the data of L bits generated by the first encoder, where $L \neq N$, and a second converter, arranged to generate second data of N bits by using a plural of the data of M bits generated by the second encoder, where $M \neq N$, and an error correction unit, arranged to selectively add an error correction check code to the first data and the second data, said error correction unit performing a common addition

processing irrespectively of the first data and the second data. Method claim 43 has been similarly amended.

Amended claims 38 and 43 are now clearly supported by the description in applicants' specification at Page 15, lines 2-16, Page 31, lines 1-6, Page 20, lines 2-21 and Page 31, line 24 to Page 32, line 13, and by FIGS. 12-14 of the applicants' Drawings. Specifically, applicants' specification discloses a first encoder (compressor 14) which encodes first digital information (the digital luminance signal) into data of L bits (shown as 4 bits). Page 15, lines 2-16. Applicants' specification also discloses a first converter (converter buffer 16), which generates data of N bits (shown as 8 bits) by using a plural of the data of L bits generated by the first encoder (compressor 14). Page 15, lines 16-20. Applicants' specification further describes a second encoder (compressor 15) and a second converter (conversion circuit 17), where the compressor 15 encodes the second digital information data (MUSE signal) and outputs data of M bits (shown as 6 bits) ($M \neq L$), and the conversion circuit 17 then converts the data of M bits into second data of N bits. Page 31, lines 1-16. Finally, an error correction unit (ECC Encoders 54-1, 54-2, 54-3) adds error correction codes to the first data and the second data and performs common addition processing irrespectively of the first or second data. Page 31, line 24 to Page 32, line 13, FIGS. 13-14.

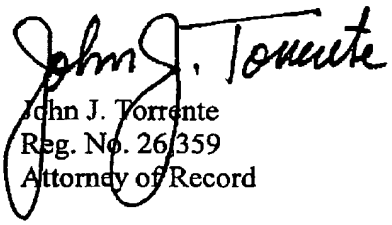
In summary, therefore, applicants' claims, as amended, are supported by an enabling disclosure. Accordingly, such claims are now in compliance with the provisions of 35 USC §112, first paragraph.

In view of the above, it is submitted that applicants' claims, as amended, comply with

all statutory requirements. Accordingly, reconsideration of the claims and passage of same to issue is respectfully requested.

Dated: May 12, 2004

Respectfully submitted,



ROBIN, BLECKER & DALEY
330 Madison Avenue
New York, New York 10017
T (212) 682-9640

John J. Torrente
Reg. No. 26,359
Attorney of Record